

4 2 Neuromorphic Architectures For Spiking Deep Neural

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4 2 Neuromorphic Architectures For

Neuromorphic Architectures

- Neuromorphic Architectures will be the next major step after von Neumann These architecture will help realize how to create parallel locality-driven architectures
- Used for what the brain is good at: compressing data into information
- Memristors will reduce power and area of these circuits by an order of magnitude or more

4.2 Neuromorphic Architectures for Spiking Deep Neural ...

Neuromorphic Architectures for Spiking Deep Neural Networks Giacomo Indiveri, Federico Corradi, and Ning Qiao Institute of Neuroinformatics, University of Zurich and ETH Zurich, Zurich, Switzerland

Neuromorphic Computing: Insights and Challenges

2 @ 500 transistors/ neuron ~10¹⁰ intersections/cm² @ 100 nm pitch ~10¹⁰ synapses /cm² Multi-Gbit/sec digital comms ~10⁶ Neurons /cm² ~5X10⁸ long range axons @ 1 Hz Neuromorphic Electronic System CROSSBAR JUNCTION CMOS SUBSTRATE LAMINAR CIRCUIT HIGH SPEED BUS ~10⁴ Neurons / cortical column Human Brain

Modular Neuromorphic VLSI Architectures for Visual Motion ...

7 Abstract Modern age intelligent systems will require extensive computational power, complex parallel process-ing units, and low-power design Biologically inspired ...

Neuromorphic Architectures

Artificial Neural Network Chips
 Early neuromorphic architectures were artificial neural network chips
 Examples:
 ETANN : (1989) Entirely analog chip that was designed for feed forward artificial neural network operation
 Ni1000 : (1996) Significantly more powerful than ...

FOUNDATIONS OF NEUROMORPHIC COMPUTING

This neuromorphic computing research and development effort explored the design and implementation of computationally intelligent computer architectures and high performance computer software algorithms

Neuromorphic Computing - GitHub Pages

Neuromorphic Computing Architectures, Models, and Applications
 The government's long history of successful investment in computing technology (probably the most valuable investment in history) is a proven case study that is relevant to the opportunity in neuromorphic computing

Low-Power Neuromorphic Hardware for Signal Processing ...

units, significantly increased parallelism and reduced energy budgets
 Such architectures have been demonstrated in neuromorphic implementations such as SpiNNaker from the University of Manchester [2], IBM's TrueNorth [3], Intel's Loihi [4], BrainScaleS built by Heidelberg

Neuromorphic Technology Developments in FET

Neuromorphic Technology Developments in FET
 Giacomo Indiveri Institute of Neuroinformatics
 Giacomo Indiveri Neuromorphic Engineering
 Channel current-voltage relationships
 "Neuromorphic Architectures for Spiking Deep Neural Networks"]

Device and System Level Design Considerations for ...

biological brain, summing nodes in neuromorphic hardware and the connections between them that store the weights are referred as neurons and synapses, respectively
 Device and System Level Design Considerations for Analog-Non-Volatile-Memory Based Neuromorphic Architectures
 S Burc Eryilmaz, Duygu Kuzum+, Shimeng Yu#, H-S Philip Wong*

MEMRISTOR-BASED COMPUTING ARCHITECTURE: DESIGN ...

Neuromorphic computing architectures imitate natural neurobiological processes by mimicking the highly parallelized computing architecture of the biological brain
 To real- computer architectures [2-3]
 Developing a neuromorphic architecture at the chip level by mimicking biological systems is another important direction
 However, a

Neuromorphic Computing: From Materials to Systems ...

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Visual Pattern Extraction Using Energy-Efficient "2-PCM ...

2206 IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL 59, NO 8, AUGUST 2012
 Visual Pattern Extraction Using Energy-Efficient "2-PCM Synapse" Neuromorphic Architecture

ON NEUROMORPHIC ARCHITECTURES FOR EFFICIENT, ...

ON NEUROMORPHIC ARCHITECTURES FOR EFFICIENT, ROBUST, AND ADAPTABLE AUTONOMY IN LIFE DETECTION AND OTHER DEEP SPACE MISSIONS
 J Tani¹, G Ruvkun², M T Zuber¹ and C E Carr¹⁻²
¹MIT Department of Earth, Atmospheric and Planetary Sciences, Cambridge, MA,
²Massachusetts General Hospital, Department of Molecular Biology, Boston, MA

Integration of nanoscale memristor synapses in ...

itself [1,2] Neuro-computing has been very popular in the past [3,4], eventually leading to the development of abstract artificial neural networks implemented on digital computers, useful for solving a wide variety of practical problems [5-9] However, the field of neuromorphic engineering is a much younger one [10]

Neuromorphic architectures with electronic synapses

Neuromorphic architectures with electronic synapses Sukru Burc Eryilmaz¹, Siddharth Joshi², Emre Neftci³, Weier Wan¹ Gert Cauwenberghs², H-S Philip Wong¹ ¹Department of Electrical Engineering and Stanford SystemX Alliance, Stanford University, Stanford, CA USA ²Department of Electrical and Computer Engineering, University of California San Diego, San Diego, CA USA

NEUROMORPHIC COMPUTING: THE POTENTIAL FOR HIGH ...

Neuromorphic-Inspired Architectures The von Neumann architecture ² is the basic building block The logic cores operate sequentially by transferring data to and from an external memory unit and the central processing unit (CPU) This energy-intensive storage process, known as the “von

CMOS and Memristor Technologies for Neuromorphic ...

CMOS and Memristor Technologies for Neuromorphic Computing Applications by Jeff KY Sun ²) Neuromorphic Computing Principles architectures (ie other than the von Neumann architecture) eventually will be needed Among these, a promising candidate is the artificial neural network and associated neuromorphic

Towards Neuromorphic Learning Machines Using Emerging ...

² Neuromorphic Computing and Emerging Devices ²¹ Digital Neuromorphic Platforms Recent progress in neuromorphic hardware has led to development of asynchronous event-driven, as opposed to synchronous or clock-driven, integrated circuits (ICs) that process and communicate information using spatio-temporal voltage spike signals

A Generic Architecture for Wafer-Scale Neuromorphic Systems

neuromorphic architectures The pin-outs of conventional integrated-circuit packages do not provide enough fan-out capability to permit the implementation of these highly connectionist architectures But, since wafer-scale integrated (1/29ds' 19ds' 2 9ds' 4 9cJ The configuration of the transistors determines the conductances